AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (withdrawn) A method for manufacturing an integrated semiconductor device, the method comprising: providing a semiconductor element having a perforation extending along a central axis of said element, thereby defining a central channel inside said element; and processing an inner surface of said perforation via the central channel to form features of the semiconductor device to be manufactured on said inner surface.

2. (withdrawn) The method of claim 1, wherein the processing comprises patterning said inner surface in accordance with the features of the semiconductor device.

3. (withdrawn) The method of claim 1, wherein the processing comprises applying to said inner surface material deposition and material removal processes.

4. (withdrawn) The method of claim 1, wherein the processing comprises applying to said inner surface a lithography process.

5. (withdrawn) The method of claim 1, wherein the processing comprises applying to said inner surface an etching process.

6. (withdrawn) The method of claim 1, wherein the processing comprises applying to said inner surface a surface polishing process.

7. (withdrawn) The method of claim 3, wherein the material deposition process includes a chemical vapor deposition.

8. (withdrawn) The method of claim 3, wherein the material deposition process includes a physical vapor deposition.

9. (withdrawn) The method of claim 3, wherein the material deposition process includes electroplating.

10. (withdrawn) The method of claim 3, wherein the material deposition process includes ion implantation.

11. (withdrawn) The method of claim 3, wherein the material removal process includes etching.

12. (withdrawn) The method of claim 3, wherein the material removal process includes chemical mechanical polishing.

13. (withdrawn) The method of claim 1, wherein said processing comprises supplying processing media into the sealed central channel.

14. (withdrawn) The method of claim 1, wherein said processing comprises flowing processing media through the central channel.

15. (withdrawn) The method of claim 1, wherein said processing comprises locating a central probe in said central channel so as to extend along the central channel.

16. (withdrawn) The method of claim 15, wherein said central probe has a cross section substantially identical to that of said perforation.

17. (withdrawn) The method of claim 15, wherein said central probe has a cross section substantially smaller than that of said perforation.

18. (withdrawn) The method of claim 15, comprises providing a relative displacement between the central probe, while in said perforation, and the semiconductor element.

19. (withdrawn) The method of claim 18, wherein the relative displacement comprises revolution of at least one of the central probe and the semiconductor element about said central axis.

20. (withdrawn) The method of claim 18, wherein said relative displacement comprises back and forward movement of at least one of the central probe and the semiconductor element along said axis.

21. (withdrawn) The method of claim 15, wherein said central probe has a plurality of perforations for supplying therethrough a processing medium towards the inner surface of the semiconductor element.

22. (withdrawn) The method of claim 15, wherein said central probe has a radiating element, the method comprising providing a relative displacement between the central probe and

the semiconductor element to thereby apply radiation to a plurality of locations on said inner surface.

23. (withdrawn) The method of claim 22, comprising synchronizing the relative displacement and the operation of the radiation element.

24. (withdrawn) The method of claim 15, wherein said central probe has a plurality of radiating elements arranged in a spaced-apart relationship along an axis parallel to the central axis to thereby apply radiation to spaced-apart locations on said inner surface.

25. (withdrawn) The method of claim 24, wherein the spacing between the radiating elements corresponds to a spacing between two locally adjacent semiconductor elements.

26. (withdrawn) The method of claim 22, wherein the radiating element is configured for generating one of the following: a light beam, an electron beam, an X-ray.

27. (withdrawn) The method of claim 24, wherein the radiating element is configured for generating one of the following: a light beam, an electron beam, an X-ray.

28. (withdrawn) The method of claim 24, wherein the central probe comprises an optical fiber having a plurality of perforations or spots in its cladding layer, said perforations or spots being arranged in the spaced-apart relationship thus presenting said plurality of radiating elements, respectively.

29. (withdrawn) The method of claim 24, wherein the central probe comprises a plurality of optical fibers accommodated such that their distal ends are arranged in the spaced-apart relationship thus presenting said plurality of radiating elements, respectively.

30. (withdrawn) The method of claim 24, comprising passing a plurality of light beams propagating through said radiating elements towards said locations through light directing elements, respectively.

31. (withdrawn) The method of claim 30, wherein the light directing element includes an annular aperture.

32. (withdrawn) The method of claim 29, comprising a plurality of light directing elements located at the distal ends of the fibers, respectively.

33. (withdrawn) The method of claim 32, wherein each of the light directing elements directs a light beam existing from the respective distal end along an axis oriented at 90 degrees to the fiber axis.

34. (withdrawn) The method of claim 32, wherein the light directing element includes an annular aperture.

35. (withdrawn) The method of claim 1, wherein said semiconductor element has the substantially circular perforation.

36. (withdrawn) The method of claim 1, wherein said semiconductor element has a ring-like cross section.

37. (withdrawn) The method of claim 1, wherein said semiconductor element is a stack of coaxially aligned sub-elements, each having a substantially planar surface by which it faces the adjacent sub-element and having the perforation, the coaxially aligned perforations defining the common central channel.

38. (withdrawn) The method of claim 1, comprising providing contact elements on a butt-end substantially flat surface of the semiconductor element.

39. (withdrawn) The method of claim 38, wherein the contact elements are made as perforations in said butt-end substantially flat surface for containing an electrically conductive material.

40. (withdrawn) The method of claim 38, comprising providing conducting leads between the contact elements and said inner surface of the semiconductor element.

41. (withdrawn) The method of claim 37, comprising configuring some of the sub-elements so as to be a connecting sub-element for its two adjacent sub-elements.

42. (withdrawn) The method of claim 41, wherein the connecting sub-element is a semiconductor or insulator.

43. (withdrawn) The method of claim 41, wherein the connecting sub-element has an array of perforations in its substantially flat surfaces for connecting said two adjacent sub-elements to each other through said perforations in the connecting sub-element.

44. (currently amended) An integrated semiconductor device manufactured by the method ~~of Claim 1~~ comprising:

providing a semiconductor element having a perforation extending along a central axis of said element, thereby defining a central channel inside said element;

processing an inner surface of said perforation via the central channel to form features of the semiconductor device including electronic elements to be manufactured on said inner surface; and

providing contact elements on substantially flat surface of a butt-end of the semiconductor element, the contact elements being connected to said inner surface.

45. (currently amended) An integrated semiconductor device comprising:

a semiconductor element having a perforation extending along a central axis of said semiconductor element ~~, an inner surface of said perforation being patterned in accordance with features of the semiconductor device~~ and defining an inner surface of said semiconductor element, said inner surface carrying electronic elements; and

contact elements arranged on a substantially flat surface of a butt-end of the semiconductor element, the contact elements being connected to said inner surface.

46. (original) The device of Claim 45, being configured such that its height is smaller than its width.

47. (original) The device of Claim 45, wherein said perforation has a substantially circular cross section.

48. (original) The device of Claim 45, wherein said semiconductor element has a substantially ring-like cross section.

49. (Canceled).

50. (currently amended) The device of Claim ~~49~~ 45, wherein said contact elements are configured as perforations in said butt-end substantially flat surface for containing an electrically conductive material.

51. (currently amended) The device of Claim 50, comprising conducting leads configured for the connecting of said contact elements to said inner surface of the semiconductor element.

52. (original) The device of Claim 45, comprising a stack of coaxially aligned sub-elements, each having a substantially planar surface by which it faces the adjacent sub-element and having the perforation, the perforations of said sub-element being coaxially aligned to define a common inner channel of the device.

53. (original) The device of Claim 45, comprising an alignment mark.

54. (original) The device of Claim 53, wherein the alignment mark is located on an outer surface of the semiconductor element.

55. (original) The device of Claim 45, comprising a cooling channel constituted by said perforation.

56. (original) An electronic circuit comprising at least two semiconductor devices, each configured as the device of Claim 45, said at least two semiconductor devices being coaxially

mounted in a stack, each of the semiconductor devices having a substantially planar surface by which it faces the adjacent device.

57. (currently amended) The circuit of Claim 56, wherein said at least two semiconductor devices have different ~~features~~ electronic elements.

58. (original) The circuit of Claim 56, comprising a cooling channel constituted by said perforation.

59. (currently amended) An integrated circuit comprising a semiconductor structure in the form of a plurality of perforated semiconductor elements arranged such that the perforations in the elements are aligned along an axis of the stack thereby defining a common perforation extending along the stack, said common perforation defining an inner surface of ~~said common perforation being patterned in accordance with features of the integrated circuit~~ said semiconductor structure, said inner surface carrying electronic elements, said semiconductor elements including contact elements arranged on a substantially flat surface of a butt-end of each semiconductor element, the contact elements being connected to said inner surface.

60. (currently amended) An integrated semiconductor device comprising a ring-like semiconductor element, an inner surface of said ring-like element ~~being patterned in accordance with features of the semiconductor device~~ carrying electronic elements, said ring-like semiconductor element including contact elements arranged on a substantially flat surface of a butt-end of said ring-like semiconductor element, the contact elements being connected to said inner surface.

61. (currently amended) An electronic circuit comprising a stack of ring-like semiconductor elements aligned along a central axis of the stack, an inner surface of the stack ~~being patterned in accordance with features of the electronic circuit~~ carrying electronic elements, said ring-like semiconductor elements including contact elements arranged on a substantially flat surface of a butt-end of each ring-like semiconductor element, the contact elements being connected to said inner surface.

62. (withdrawn) A method of manufacturing a ring-like semiconductor device, the method comprising providing a ring-like semiconductor element; and applying a lithography process to an inner surface of the ring like semiconductor element to thereby define features of the semiconductor device.

63. (withdrawn) A probe for use in manufacturing a semiconductor device on an inner surface of a perforated semiconductor element, the probe being configured for passing therethrough a processing medium and for being insertable in the perforation in the semiconductor element, the probe comprising at least one outlet of said medium, to thereby supply said medium though said at least one output towards the inner surface of the perforated semiconductor element.

64. (withdrawn) The probe of claim 63, wherein said medium is liquid.

65. (withdrawn) The probe of claim 63, wherein said medium is gas.

66. (withdrawn) The probe of claim 53, wherein said medium is certain radiation.

67. (withdrawn) The probe of claim 66, wherein said certain radiation includes one of the following: a light beam, a charged particles beam, an X-ray.

68. (withdrawn) The probe of claim 63, comprising the single outlet, a relative displacement between said probe and said semiconductor element resulting in that said medium is supplied to spaced-apart locations on said inner surface.

69. (withdrawn) The probe of claim 63, comprising a plurality of said outlets arranged in a spaced-apart relationship along the probe, thus allowing for supplying said medium to spaced-apart locations on said inner surface.

70. (withdrawn) An optical probe for use in manufacturing at least one semiconductor device on an inner surface of a perforated semiconductor structure, the probe having a tubular geometry of a diameter so as to be insertable in the perforation in the semiconductor element, and comprising a plurality of radiating elements arranged in a spaced-part relationship along the probe, the probe being operable to irradiate spaced-apart locations on the inner surface of the perforated semiconductor element.

71. (withdrawn) The probe of claim 70, comprising an optical fiber having a plurality of perforations or spots in its cladding layer, said perforations or spots being arranged in the spaced-apart relationship thus presenting said plurality of radiating elements, respectively.

72. (withdrawn) The probe of claim 70, comprising a plurality of optical fibers accommodated such that their distal ends, to be located inside said perforation in the semiconductor element, are arranged in the spaced-apart relationship thus presenting said plurality of radiating elements, respectively.

73. (withdrawn) The probe of claim 70, wherein the spacing between the radiating elements corresponds to a spacing between two adjacent perforated semiconductor elements in a stack of semiconductor elements forming said semiconductor structure.

74. (withdrawn) The probe of claim 70, comprising a plurality of light directing elements, each accommodated in a path of a light beam coming from the respective one of said radiating elements.

75. (withdrawn) The probe of claim 74, wherein the light directing element includes an annular aperture.

76. (withdrawn) The probe of claim 72, comprising a plurality of light directing elements located at the distal ends of the fibers, respectively, each of the light directing elements directing a light beam existing from the respective distal end along an axis oriented at 90 degrees to the fiber axis.

77. (withdrawn) A processing system for use in manufacturing at least one semiconductor device on an inner surface of a perforated semiconductor structure, the system being configured for supplying a selective processing medium, from a plurality of different media, into the perforation in the semiconductor element, the probe comprising an inlet arrangement including a valve assembly configured for selectively connecting a selective one of medium supply units, from a plurality of such units, to the perforation.

78. (withdrawn) The system of claim 77, configured for flowing the processing medium through the perforation in the semiconductor structure, the system comprising an outlet

arrangement accommodated at other side of the perforation opposite to the inlet arrangement and comprising a valve arrangement configured for selectively connecting the inside of said perforation towards either one of medium recycle and waste channels.